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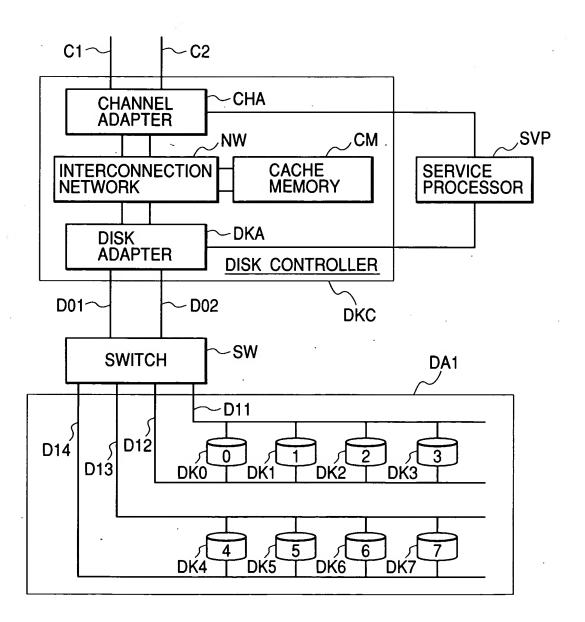
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FIG. 1



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FIG. 2
CONFIGURATION OF CHANNEL ADAPTER CHA

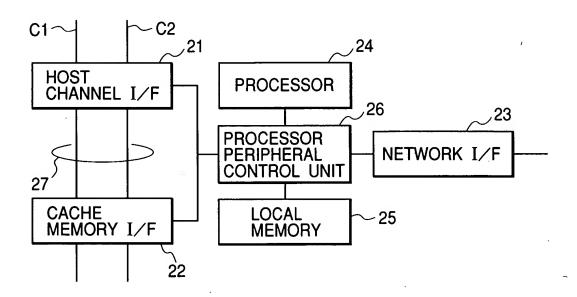
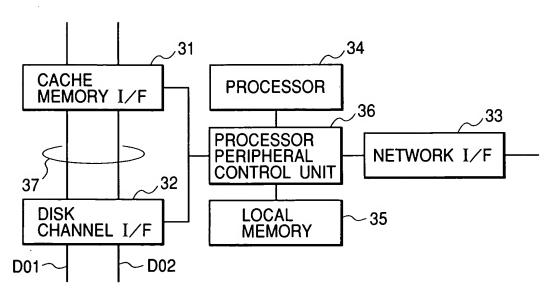


FIG. 3
CONFIGURATION OF DISK ADAPTER DKA



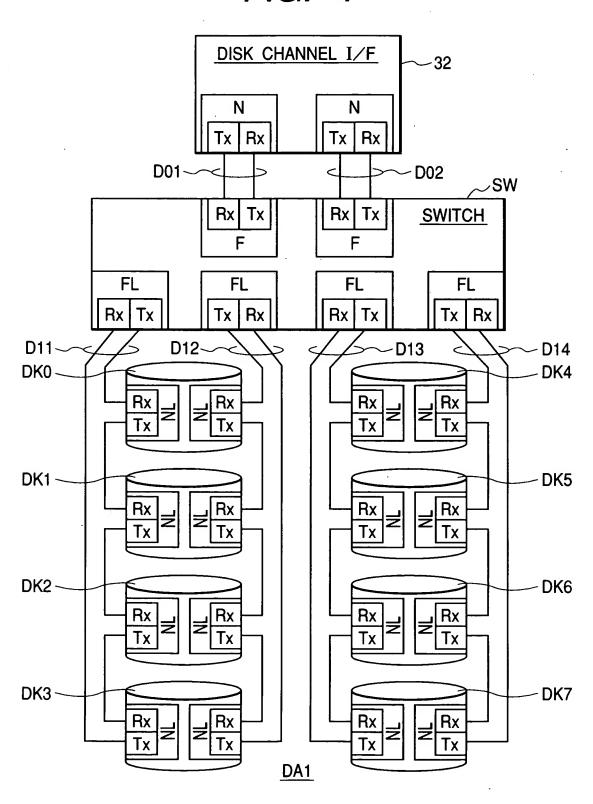
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FIG. 4

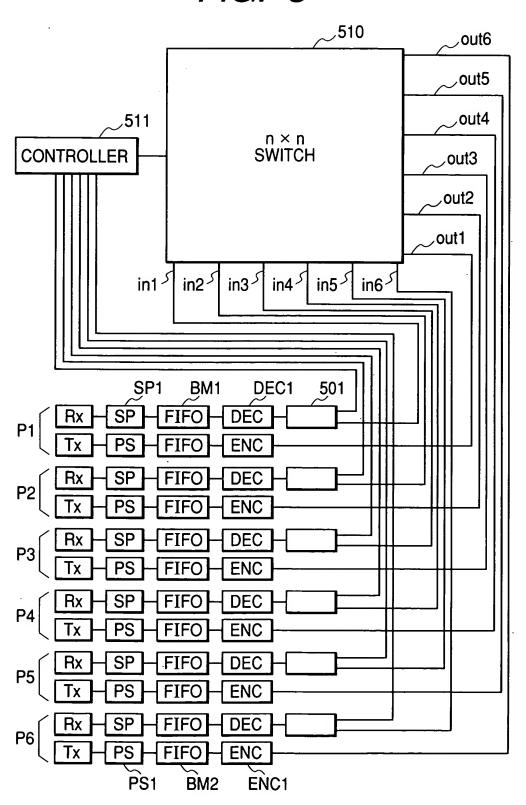


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FIG. 5



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FIG. 6

		_~ 601		602	603			
	WITHOUT	FAILURE	WHEN "a" FA	PORT ILS	WHEN PORT "b" FAILS			
DRIVE NO.	Read	Write	Read	Write	Read	Write		
0	PID_0. a	PID_0. b	PID	PID_0. b		_0. a		
1	PID_1. a	P.ID_1. b	PID_1. b		PID_1. a			
2	PID_2. a	PID_2. b	PID	_2. b	PID_2. a			
3	PID_3. a	PID_3. b	PID_3. b		PID_3. a			
4	PID_4. a	PID_4. b	PID	_4. b	PID_4. a			
5	PID_5. a	PID_5. b	PID	PID_5. b		PID_5. b PID_9		_5. a
6	PID_6. a	PID_6. b	PID	PID_6. b		PID_6. b PID		_6. a
7	PID_7. a	PID_7. b	PID	PID_7. b PID		_7. a		
1	ll							

FIG. 7

₂701

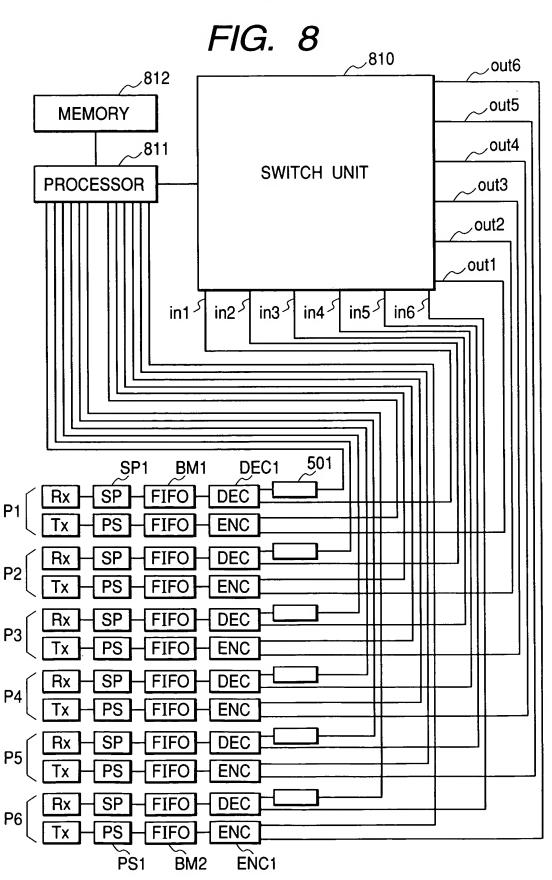
		~ 101					
	WITHOUT	FAILURE	WHEN "a" FA	PORT ILS	WHEN PORT "b" FAILS		
DRIVE NO.	Read	Write	Read	Write	Read	Write	
0	PID_0. a	PID_0.b	PID	_0. b	PID_0. a		
1	PID_1. b	PID_1. a	PID	_1. b	PID_1. a		
2	PID_2. a	PID_2. b	PID	_2. b	PID_2. a		
3	PID_3. b	PID_3. a	PID	_3. b	PID_3. a		
4	PID_4. a	PID_4. b	PID	_4. b	PID_4. a		
5	PID_5. b	PID_5. a	PID	_5. b	PID	_5. a	
6	PID_6. a	PID_6. b	PID_6. b		PID	_6. a	
7	PID_7. b	PID_7. a	PID	_7. b	PID_7. a		

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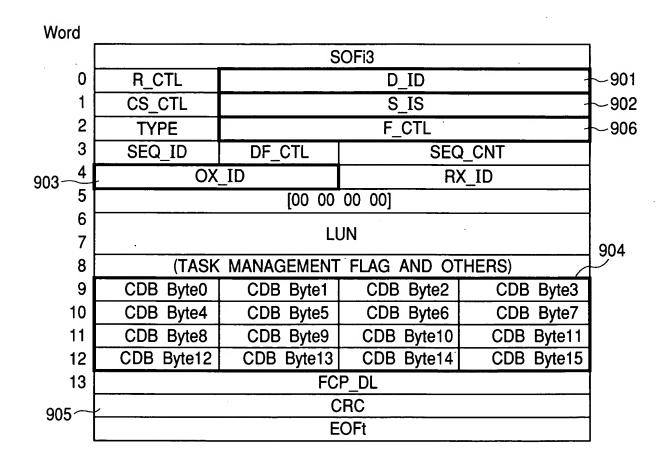


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FIG. 9

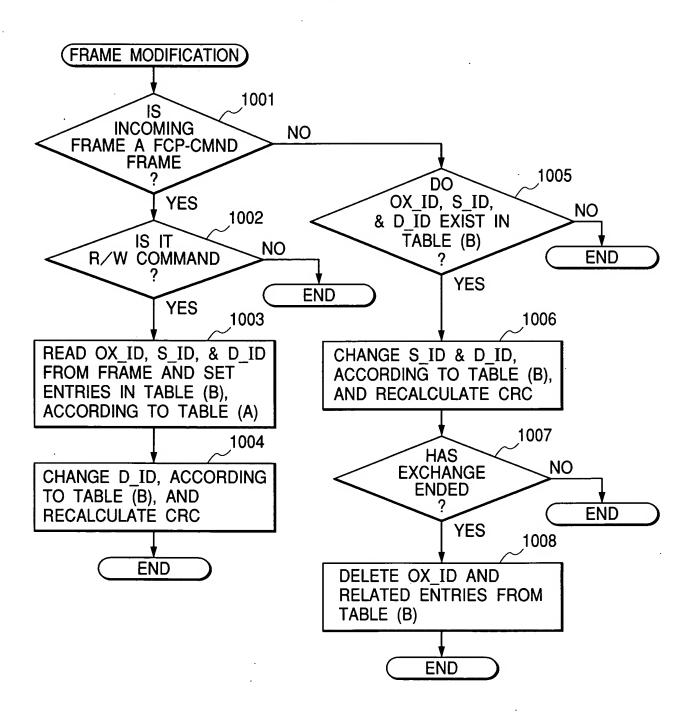


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FIG. 10



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WITHOUT CHANGE WITHOUT CHANGE AFTER MODIFICATION FIG. 11B WITHOUT CHANGE WITHOUT CHANGE S_ID BEFORE | MODIFICATION | ർ Φ ൯ ൯ 0x03F2 0x03F2 0x03F3 104~\ OX ID 0x03F3 1109~

	03	_											 	
A	11021103	Write	PID_0. b	PID_0.b	PID_1.b	PID_1. b	PID_2. b	PID_2. b	PID_3. b	PID_3. b	PID_4. b	PID_4. b		
11A	11	Read	PID_0. a	PID_0. a	PID_1. a	PID_1. a	PID_2. a	PID_2. a	PID_3. a	PID_3. a	PID_4. a	PID_4. a		
FIG	1101	Drive Port_ID	PID_0. a	PID_0. b	PID_1.a	PID_1.b	PID_2. a	PID_2. b	PID_3. a	PID_3.b	PID_4. a	PID_4.b		

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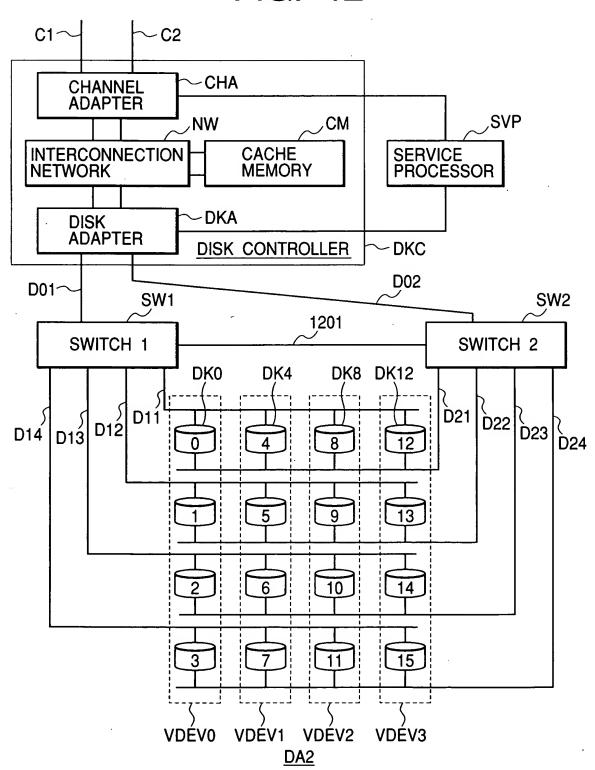
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FIG. 12



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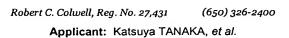
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FIG. 13

1301			·	1302		1303		1304	
		W	ITHOUT FA	ILURE	WH FAI	EN SW1 LS	WHEN SW2 FAILS		
DRIVE NO.	VDEV	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port	
0			PID_0. a	PID_0. b		PID_0. b		PID_0. a	
1	0	0	PID_1. a	PID_1. b	1	PID_1.b	0	PID_1. a	
2		U	PID_2. a	PID_2. b	'	PID_2. b		PID_2. a	
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a	
4			PID_4. a	PID_4. b		PID_4. b	0	PID_4. a	
5	1	0	PID_5. a	PID_5. b	1	PID_5. b		PID_5. a	
6	'	U	PID_6. a	PID_6. b		PID_6. b		PID_6. a	
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a	
8			PID_8. a	PID_8. b		PID_8. b	0	PID_8. a	
9	2	0	PID_9. a	ID_9. a PID_9. b	1	PID_9. b		PID_9. a	
10		U	PID_10. a	PID_10. b	•	PID_10. b		PID_10. a	
11		_	PID_11. a	PID_11. b		PID_11. b		PID_11. a	
12		, .	PID_12. a	PID_12. b		PID_12. b		PID_12. a	
13	3	0	PID_13. a	PID_13. b	1	PID_13. b	0	PID_13. a	
14	٦	U	PID_14. a	PID_14. b	. •	PID_14. b	U	PID_14. a	
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a	



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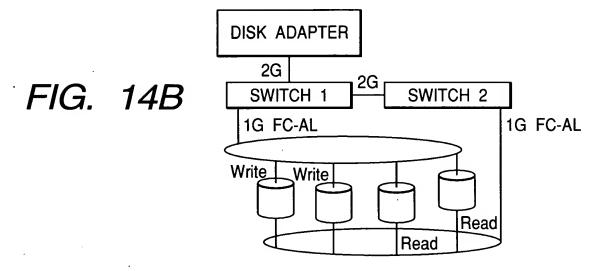
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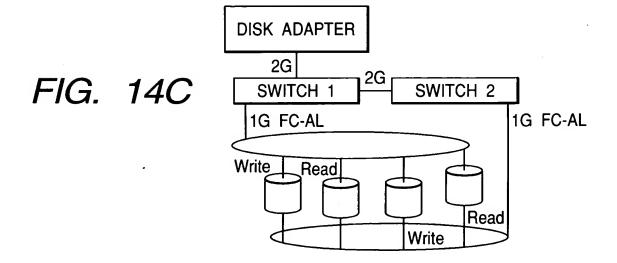
FIG. 14A

DISK ADAPTER

IG FC-AL

Write Write Read Read





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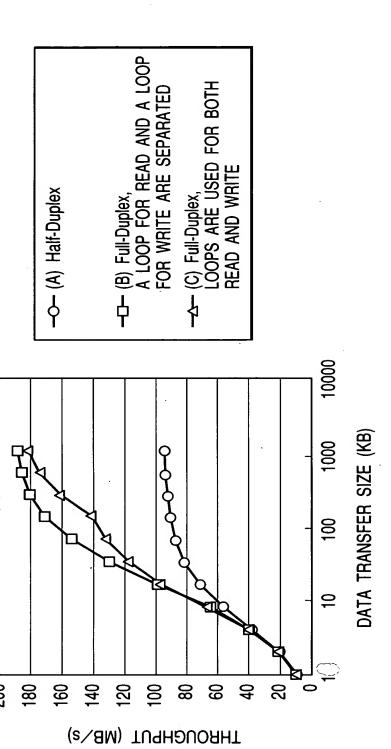


FIG. 15

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FIG. 16

<u>_</u>1601

~ 1001										
		W	/ITHOUT FA	ILURE	WH FAI	EN SW1 LS	WHEN SW2 FAILS			
DRIVE NO.	VDEV	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port		
0			PID_0. a	PID_0. b		PID_0. b		PID_0. a		
1	0	0	PID_1. a	PID_1. b	1	PID_1. b	0	PID_1. a		
2		U	PID_2. a	PID_2. b	•	PID_2. b	U	PID_2. a		
3			PID_3. a	PID_3. b		PID_3. b		PID_3. a		
4			PID_4. a	PID_4. b		PID_4. b	0	PID_4. a		
5	1	1	PID_5. a	PID_5. b	1	PID_5. b		PID_5. a		
6	'	ļ	PID_6. a	PID_6. b		PID_6. b		PID_6. a		
7			PID_7. a	PID_7. b		PID_7. b		PID_7. a		
8		•	PID_8. a	PID_8. b		PID_8. b	Ö	PID_8. a		
9	2	0	PID_9. a	PID_9. b	1	PID_9. b		PID_9. a		
10	2	U	PID_10. a	PID_10. b	. 1	PID_10. b		PID_10. a		
11			PID_11. a	PID_11. b		PID_11. b	:	PID_11. a		
12			PID_12. a	PID_12. b		PID_12. b		PID_12. a		
13	3	1	PID_13. a	PID_13. b	1	PID_13. b	n	PID_13. a		
14		1	PID_14. a	PID_14. b	'	PID_14. b	0	PID_14. a		
15			PID_15. a	PID_15. b		PID_15. b		PID_15. a		
					-					
				,						

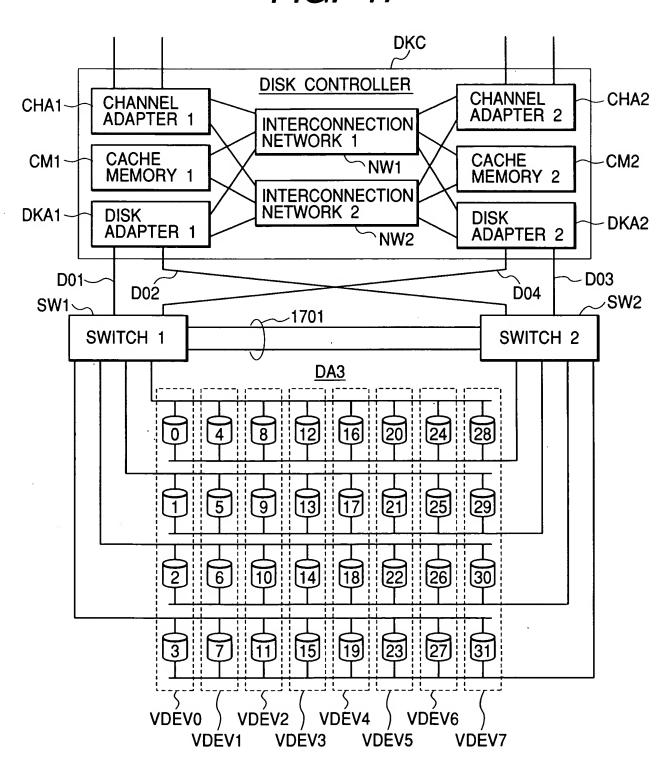
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FIG. 17



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FIG. 18 1801

	7.	10	1801																		
			WITHOUT FAILURE			WH FAI	EN SW1 LS	WHEN SW2 FAILS													
DRIVE NO.	VDEV	DKA NO.	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R/W Drive Port												
0				PID_0. a	PID_0. b		PID_0. b		PID_0. a												
1	0	0	0	PID_1. a	PID_1. b	1	PID_1.b	0	PID_1. a												
2			U	PID_2. a	PID_2. b	'	PID_2. b	U	PID_2. a												
3				PID_3. a	PID_3. b		PID_3. b		PID_3. a												
4				PID_4. a	PID_4. b		PID_4. b		PID_4. a												
5	1	1	0	PID_5. a	PID_5. b	0	PID_5. b	1	PID_5. a												
6	'	1	U	PID_6. a	PID_6. b	U	PID_6. b	'	PID_6. a												
7				PID_7. a	PID_7. b		PID_7. b		PID_7. a												
8				PID_8. a	PID_8. b		PID_8. b		PID_8. a												
9	2	0	1	PID_9. a	PID_9. b	1	PID_9. b	0	PID_9. a												
10	۷	U	. '	PID_10. a	PID_10. b	'	PID_10. b	U	PID_10. a												
11				PID_11. a	PID_11. b		PID_11. b		PID_11. a												
12			_	PID_12. a	PID_12. b		PID_12. b	8	PID_12. a												
13	3	1	1	PID_13. a	PID_13. b		PID_13. b	1	PID_13. a												
14	٥	l		PID_14. a	PID_14. b		PID_14. b		PID_14. a												
15				PID_15. a	PID_15. b		PID_15. b		PID_15. a												
16				PID_16. a	PID_16. b		PID_16. b		PID_16. a												
17	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PID_17. a	PID_17. b		PID_17. b	0	PID_17. a
18	*															0 PID_18. a PID_18. b	•	PID_18. b		PID_18. a	
19				PID_19. a	PID_19. b		PID_19. b		PID_19. a												
20				PID_20. a	PID_20. b		PID_20. b		PID_20. a												
21	5	1	0	PID_21. a	PID_21. b	0	PID_21. b	1	PID_21. a												
22	5	•	U	PID_22. a	PID_22. b		PID_22. b	'	PID_22. a												
23				PID_23. a	PID_23. b		PID_23. b		PID_23. a												
24				PID_24. a	PID_24. b		PID_24. b		PID_24. a												
25	6	0	1	PID_25. a	PID_25. b	1	PID_25. b	0	PID_25. a												
26	0	U	'	PID_26. a	PID_26. b	'	PID_26. b	U	PID_26. a												
27				PID_27. a	PID_27. b		PID_27. b		PID_27. a												
28				PID_28. a	PID_28. b		PID_28. b		PID_28. a												
29	7	1	1	PID_29. a	PID_29. b	0	PID_29. b	1	PID_29. a												
30	'	ı	•	1		'	1	•	PID_30. a	PID_30. b]	PID_30. b] '	PID_30. a							
31				PID_31. a	PID_31. b		PID_31. b		PID_31. a												
									_												

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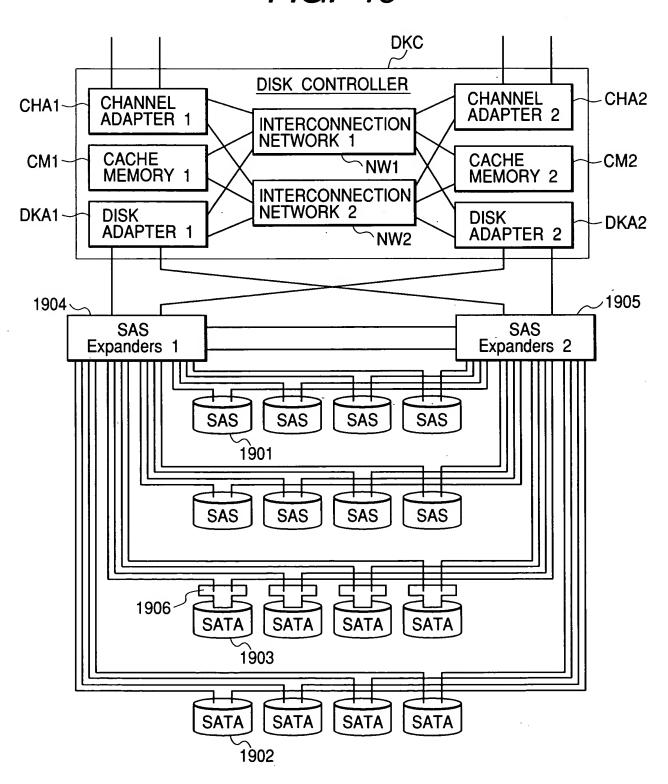
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FIG. 19



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FIG. 20

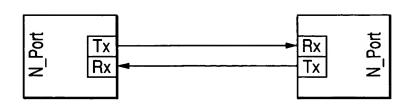


FIG. 21

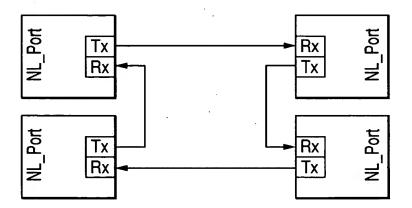
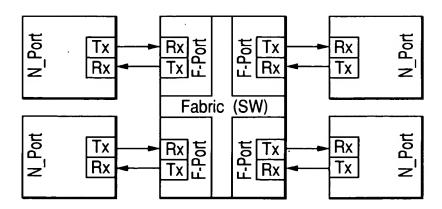


FIG. 22



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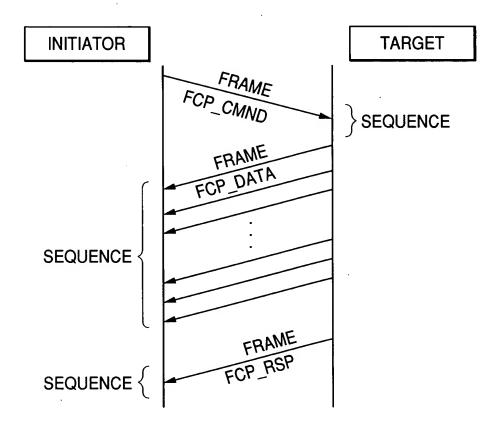
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FIG. 23



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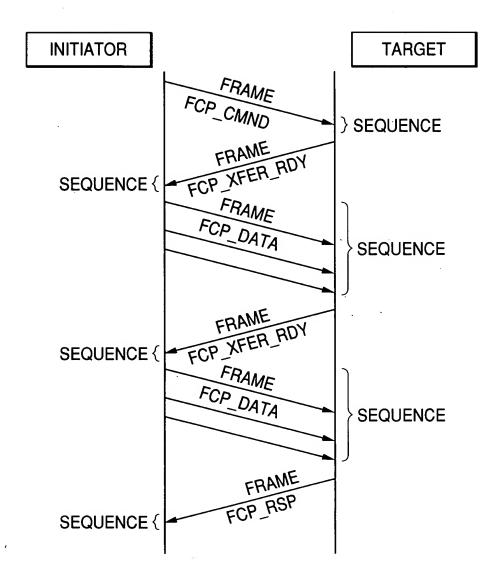
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FIG. 24



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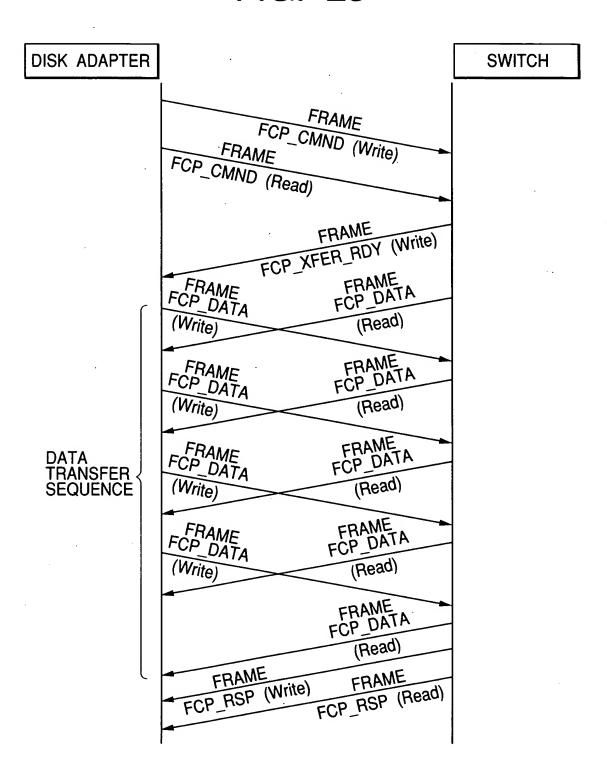
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FIG. 25



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FIG. 26

	MUEN ONG MUEN ONG																	
			W	WITHOUT FAILURE			EN SW1 LS	WHEN SW2 FAILS										
DRIVE NO.	VDEV	DKA NO.	DKA Port	Read Drive Port	Write Drive Port	DKA Port	R/W Drive Port	DKA Port	R∕W Drive Port									
0				PID_0. a	PID_0. b		PID_0. b		PID_0. a									
1	0	0	0	PID_1. b	PID_1. a	1	PID_1. b	0	PID_1. a									
2	0	U		PID_2. a	PID_2. b	1	PID_2. b	U	PID_2. a									
3				PID_3. b	PID_3. a		PID_3. b		PID_3. a									
4				PID_4. a	PID_4. b	·	PID_4. b		PID_4. a									
5	1	1	0	PID_5. b	PID_5. a	0	PID_5. b	1	PID_5. a									
6	'	I	U	PID_6. a	PID_6. b	U	PID_6. b	'	PID_6. a									
7				PID_7. b	PID_7. a		PID_7. b		PID_7. a									
8				PID_8. a	PID_8. b		PID_8. b		PID_8. a									
9	2	0	.	PID_9. b	PID_9. a		PID_9. b	_	PID_9. a									
10	2	U	1	PID_10. a	PID_10. b	1	PID_10. b	0	PID_10. a									
11				PID_11. b	PID_11. a		PID_11. b		PID_11. a									
12				PID_12. a	PID_12. b	0	PID_12. b	1	PID_12. a									
13	3	1	1	PID_13. b	PID_13. a		PID_13. b		PID_13. a									
14	ა	I	.	PID_14. a	PID_14. b		PID_14. b		PID_14. a									
15				PID_15. b	PID_15. a		PID_15. b		PID_15. a									
16		0	0	0	0	0		PID_16. a	PID_16. b		PID_16. b		PID_16. a					
17	4						0	0	0	Λ	Ω	0	PID_17. b	PID_17. a	1 .	PID_17. b	0	PID_17. a
18	*							U	PID_18. a	PID_18. b	1	PID_18. b] "	PID_18. a				
19										PID_19. b	PID_19. a		PID_19. b	1	PID_19. a			
20				PID_20. a	PID_20. b		PID_20. b		PID_20. a									
21	5	1	0	PID_21. b	PID_21. a	0	PID_21. b	4	PID_21. a									
22	,	'	"	PID_22. a	PID_22. b	U	PID_22. b	1	PID_22. a									
23				PID_23. b	PID_23. a		PID_23. b		PID_23. a									
24				PID_24. a	PID_24. b		PID_24. b		PID_24. a									
25	6	0	1	PID_25. b	PID_25. a	1	PID_25. b	0	PID_25. a									
26	0	U	'	PID_26. a	PID_26. b	1	PID_26. b	U	PID_26. a									
27				PID_27. b	PID_27. a		PID_27. b		PID_27. a									
28				PID_28. a	PID_28. b		PID_28. b		PID_28. a									
29	7	4	1	PID_29. b	PID_29. a	0	PID_29. b		PID_29. a									
30	'	'	'	'	1	'	PID_30. a	PID_30. b	U	PID_30. b	1	PID_30. a						
31				PID_31. b	PID_31. a		PID_31. b		PID_31. a									